Design rules check

ADC128S102

* the clock line as short as possible.
* analog and digital lines should cross each other at 90° to avoid crosstalk. (CROSSTALK is the coupling of energy from one channel into another channel. This is similar to Channel-toChannel Isolation, except for the sign of the data.)
* However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether
* It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines.
* In addition, the clock line should also be treated as a transmission line and be properly terminated.
* The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input.
* Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

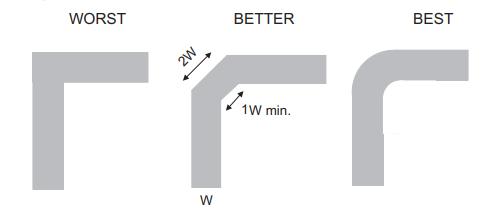
ADUM240E0/ADUM241E1

* Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for VDD1 and between Pin 15 and Pin 16 for VDD2.
* The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.
* In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized.
* Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side.

CD74HC595SM96

* When using multiple-input and multiple-channel logic devices inputs must not ever be left floating

CD74HC4051



OPA187I

* Low-ESR, 0.1-µF ceramic bypass capacitors must be connected between each supply pin and ground; place the capacitors as close to the device as possible
* To reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
* Place the external components as close to the device as possible.